PID INVESTIGATION OF BIFACIAL PERC SOLAR CELLS

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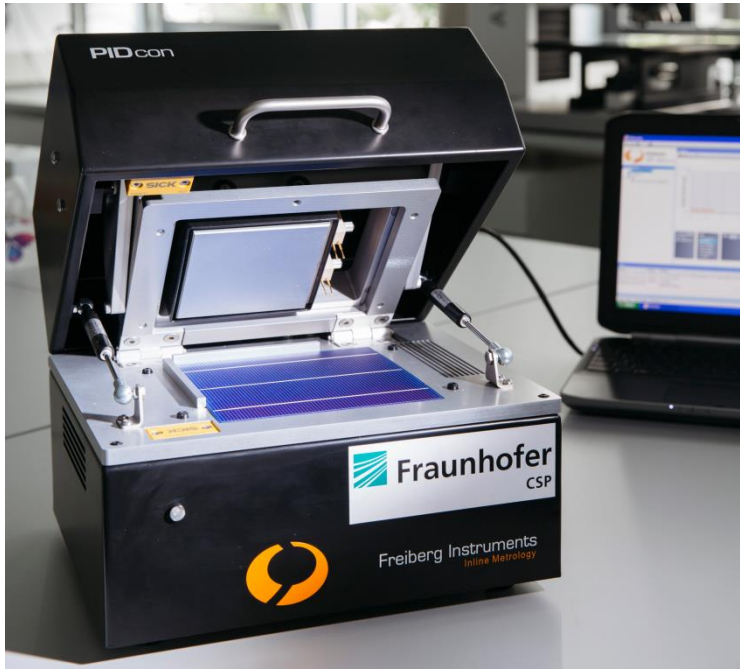
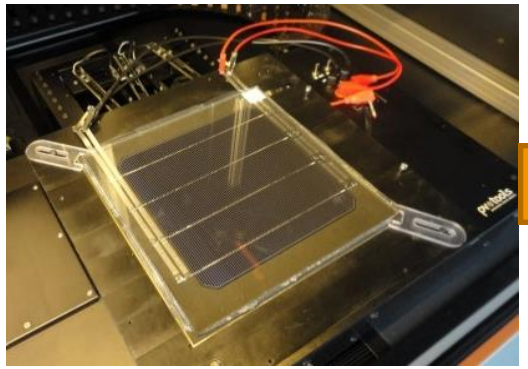


Fraunhofer CSP

→ www.PIDcon.com

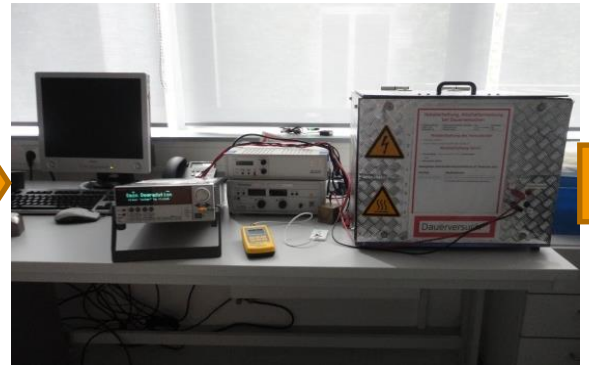
Experimental set-up

Test procedure of the PID tests



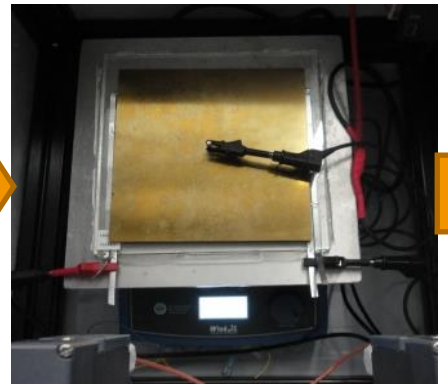
initial characterization

- measurement of IV, EL, EQE from front and rear side
- metallic chuck covered with black cloth
- temperature = 25°C



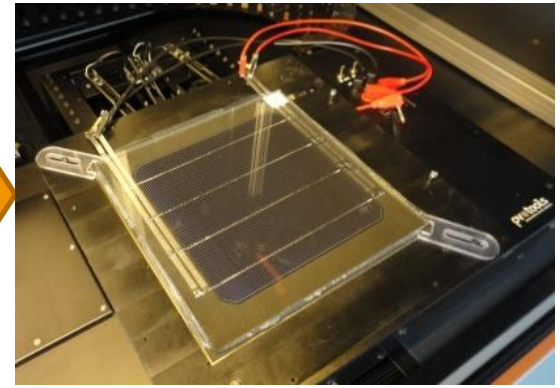
PID cell and mini-module tester

- provided temperature range 25°C to 150°C
- voltage up to ± 1 kV



mini-module in cell tester

- high voltage applied over full module area
- PID test: 24 h at 60 °C



final characterization

- like initial

Sample overview and testing conditions

Four PID stress-scenarios were tested

Samples: four glass-glass mini-modules

- 3mm float glass, both sides
- encapsulation: EVA; Avaluxe EVA-FL TL MG ARC2

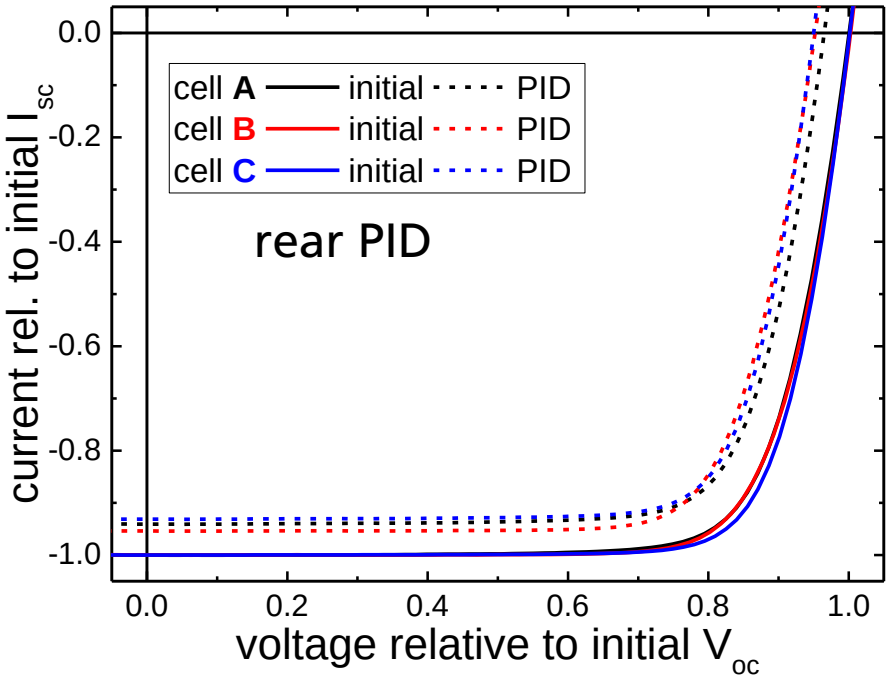
Measuring conditions

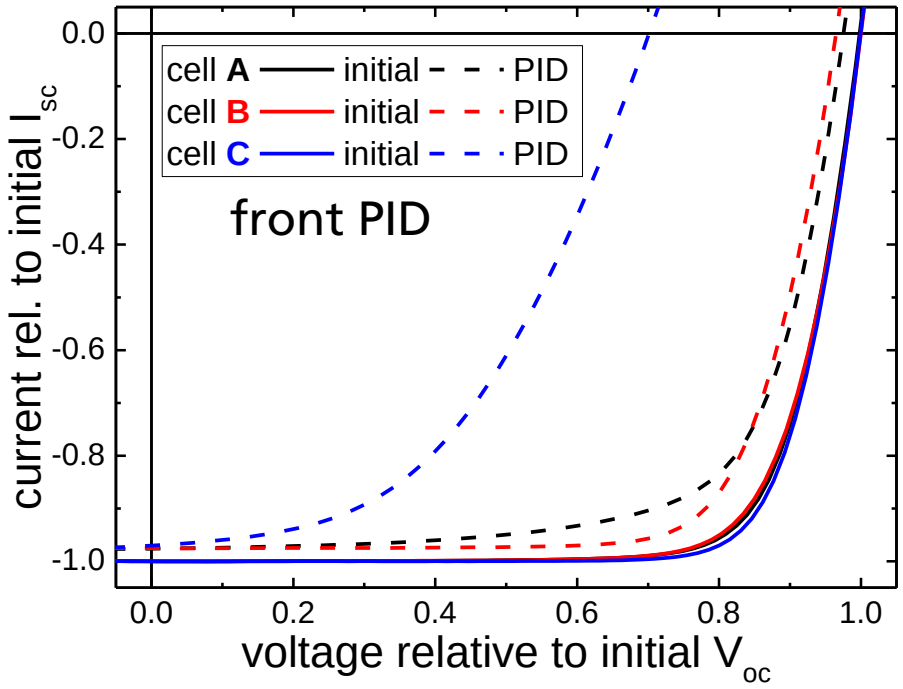
- cell on U = 0 V
- high voltage U_{PID} = +1000 V applied to the front or back side of the cell (equals outdoor conditions)
- duration 24 h
- temperature T=60°C
- new module used for each side and voltage

PID test set up: cell on ground level 0V, brass plate on high voltage U_{PID} = ± 1000 V. SMU (Keithley 2601A) used for in situ dark-I-V

PID benchmark for three different PERC+ cells

All cells are prone to PID at both sides

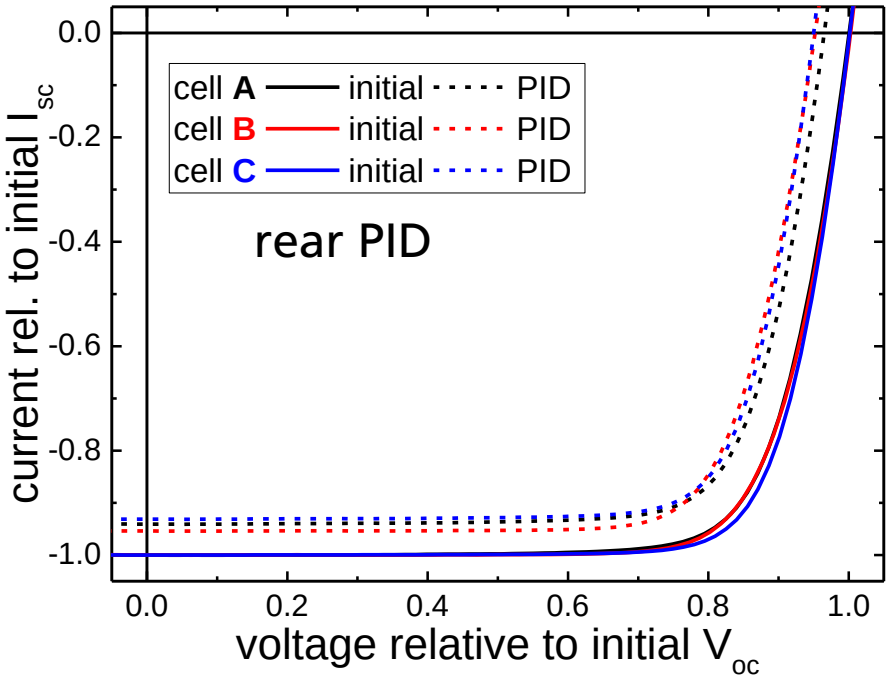




- three cell types under test: all PERC+, p-type, emitter front (3 different manufacturers)
- PID-test: 24h, 60°C, cell on 0V; glass surface on high potential
- all cells are prone to PID at the front and at back side
- rear side PID results from a de-passivation

PID benchmark for three different PERC+ cells

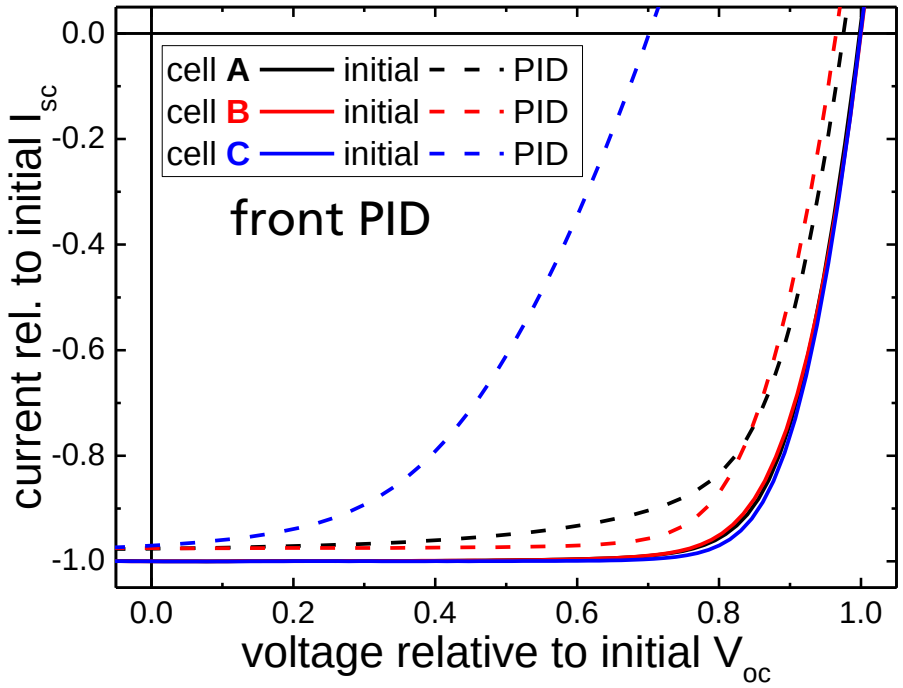
All cells are prone to PID at both sides



ΔIsc = (-5.9%, -4.6%, -6.9%)

ΔVoc = (-3.5%, -5.0%, -5.1%)

FF not affected, p-n junction not short circuited



ΔIsc = (-2.4%, -2.5%, -3%)

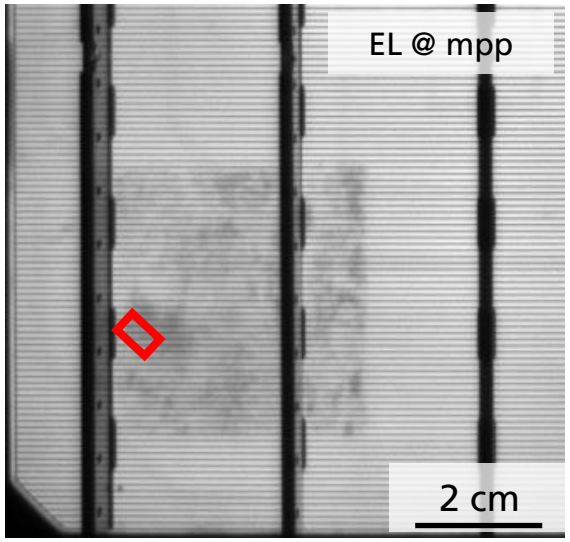
ΔVoc = (-2.3%, -3.5%, -30%)

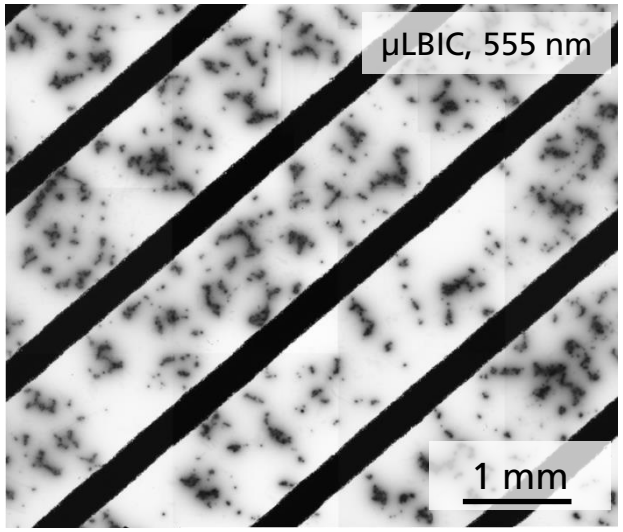
ΔFF = (-9%$_{rel}$, -1.9%$_{rel}$, -40%$_{rel}$)

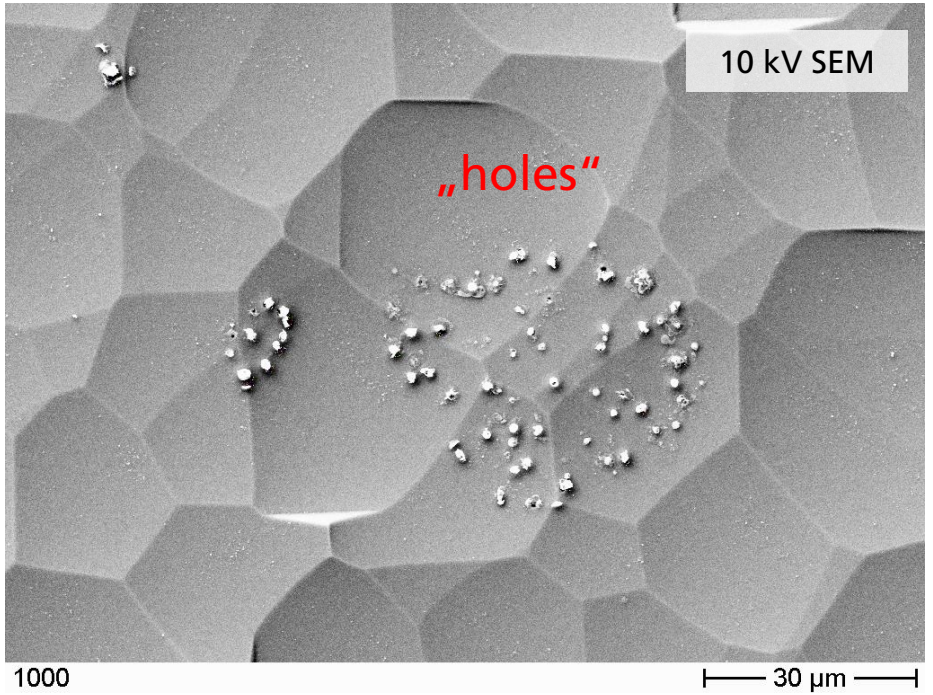
Fraunhofer CSP

PID: microscopic error image

PID can damage the cell surface







- reference areas with EVA and glass but without voltage are hole-free
- holes occur only under PID stressed area
- holes in the back surface are electrically active

Summary

key findings

- in our experiments cells suffer from a performance loss of -12.7% due to PID at the rear side
- degraded cells reveal holes in the surface of the back;
  the recombination in the surroundings of the holes is increased

outlook

- so far only few samples were studied -> material variation and statistics required
- PID recovery behavior has to be checked
- role of local impurities has to be investigated
- mechanism for the formation of passivation holes has to be clarified

→ anonymous results will be published on https://www.pidcon.com/en.html soon!

Further acitivities/cooperation

- sytematic material and process assessment in PID defect diagnostics on bifacial solar cells and modules
- PID analysis of front versus rear side tested by PIDcon tester
- bench marking www.pidcon.com
- advanced root cause analysis -> SiliconPV 2019