PID TESTING OF SOLAR CELLS

Application notes on PIDcon cell testing

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Part 1: PID of c-Si solar cells

*EL images of a mc-Si solar module before and after occurrence of PID*
Potential-induced degradation (PID) of c-Si solar cells

- PID results in a very strong power decrease of c-Si solar modules
- Massive shunting solar cells → this prevalent type of PID is called “PID-s”
- Responsible: leakage current – dependent on voltage and temperature

Leakage current path
(1) through glass/polymer (predominant)
(2) lateral through polymer foil (minor contributions)
(3) through backsheet (extraneous to PID-s)

Source: UL International Germany
Electrical model for PID

- Special glass sorts cause resistance against PID-s
- Some polymer foils cause resistance against PID-s
- Leakage current $I$ influenced by resistivity of glass and polymer

- PID-s resistance also achieved through low resistivity of SiN$_x$ layer (high refractive index)
- Voltage across SiN$_x$ layer: $V_{SiN}$ is the critical parameter

$V_{SiN} = I \cdot R_{SiN}$

Physical root cause for PID-s

- High voltage across SiN_x layer causes drift of alkali ions
- Decoration of extended defects in Si {111} planes → “stacking faults” from the SiN_x/Si interface
  - High electric conductivity of stacking faults → shunting
  - Assessment of shunt resistance $R_p$ to quantify PID-s
Part 2: Experimental setup for PIDcon cell testing
PID testing using the standard module test (for comparison)

- On module level: PID test standard available: **IEC 62804-1 TS**: "Photovoltaic (PV) modules – Test methods for the detection of potential-induced degradation – Part 1: Crystalline silicon"
- Procedure (b): Contacting surface by covering with grounded, electrically conducting electrode in controlled environment

**Parameters:**
- Module with Al foil in environmental chamber
- Temperature: 25 °C (up to 60 °C)
- Dry conditions
- Duration: 168 hours
- Voltage: 1000 or 1500 V (depending on module type)

**But:**
- Long test time
- Elaborate module manufacturing needed
- Expensive equipment/operation

→ Quick PID test on cell level attractive
**PIDcon cell test**

**Setup**

- Module-like layer stack of solar cell + polymer foil + glass between two metal electrodes
- High positive voltage at upper electrode → voltage equivalent to PID in module
- Bottom electrode (ground) is heated
- Acquisition of shunt resistance as a function of time

*Schematic of the PIDcon test setup*
PIDcon cell test

Materials

Solar cell:
- Si solar cell, minimum size 125 x 125 mm
- Front side contact grid with at least two busbars
- Original shunt resistance (before PID test) between some 10 \( \Omega \) and 15 k\( \Omega \)

Polymer foil:
- EVA foil \((d < 0.5 \text{ mm})\) with resistivity \(\sim 10^{13} \Omega \text{cm}\) (e.g. Bridgestone EVASKY)

Glass:
- Float glass, according to DIN EN 572-2, with low iron content
- Thickness: 3…4 mm
- Pieces of 10 x 10 cm\(^2\)
PIDcon cell test

Test conditions

Preparation (according to SEMI standard)*:

- Stack EVA and glass (both 10 x 10 cm, square format) on solar cell, well aligned to top electrode
- Pre-lamination of the layer stack (in-situ option): 20 min @150 °C

Standard test conditions:

- Voltage: 1000 V
- Temperature: 85 °C
- Test duration: at least 4 hours
- Dry conditions, no use of water

Part 3: Example results

Four-fold PIDcon test device at Fraunhofer CSP
Results of a PID cell test series

- PID test of three Si solar cell types at 60 °C and 1000 V
- Plot of parallel resistance (shunt) as a function of PID test time

- Initial $R_p$ value depends on cell process
- $R_p$ is reciprocal of shunting degree (very sensitive to minor current variations at high $R_p$ levels)
- Low $R_p$ means high currents through shunts (PID-shunts)

The three cell types show significant differences in the progress of shunting due to PID-s with good repeatability.
Results of a PID cell test series

- Plot of conductance (conductance = 1 / parallel resistance / stressed area)

- Conductance is proportional to current losses through shunts and (in first approx.) proportional to power loss at mpp

→ Power losses take effect first at very low $R_p$ values

Cell type ‘2 sensitive’ shows up to 6x of the power loss of cell type ‘1 sensitive’. Cell type ‘1 resistant’ exhibits no power loss due to PID-s.
Extensive PID cell test series

- PID test of the same three Si solar cell types at 85 °C and 1000 V

![Diagram showing parallel resistance over time for three cell types: M1 (multi) PID-s stable, M1 (mono) PID-s sensitive, M2 (multi) PID-s sensitive. The diagram indicates > 5% power loss after a certain time.]
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Power loss due to PID-s

Solar cell:

Equivalent circuit diagram:

Two-diode-model:
\[ I = I_{D1}(U_i) + I_{D2}(U_i) + \frac{U_i}{R_p} - I_L, \quad U_i = U - IR_s \]

Approximation: power loss \( \Delta P \) is proportional to current loss through shunts:
\[ \Delta P \approx U_{mpp} \times \frac{U_{mpp}}{R_p} \]

relative power loss:
\[ \frac{\Delta P}{P} \approx \frac{1}{I_{mpp}} \times \frac{U_{mpp}}{R_p} \]