PID TESTING OF SOLAR CELLS

Application notes on PIDcon cell testing

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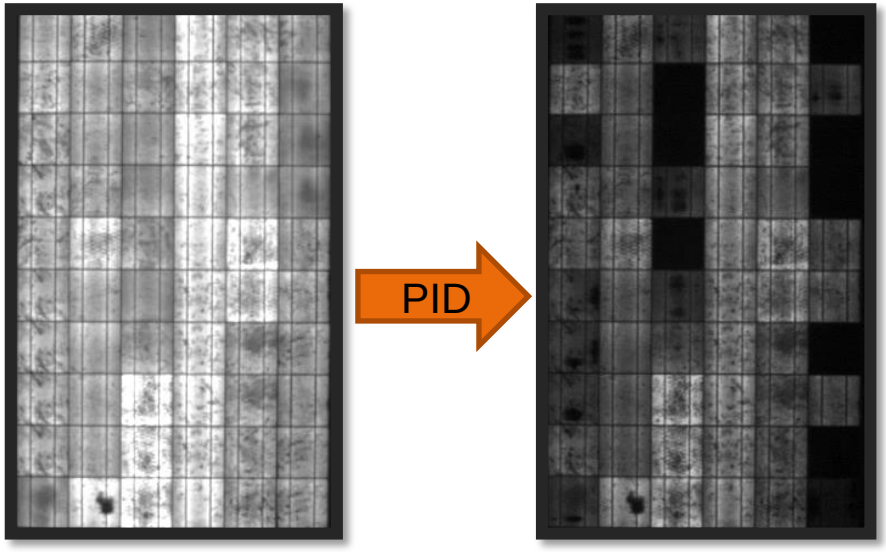
Part 1: PID of c-Si solar cells



EL images of a mc-Si solar module before and after occurence of PID

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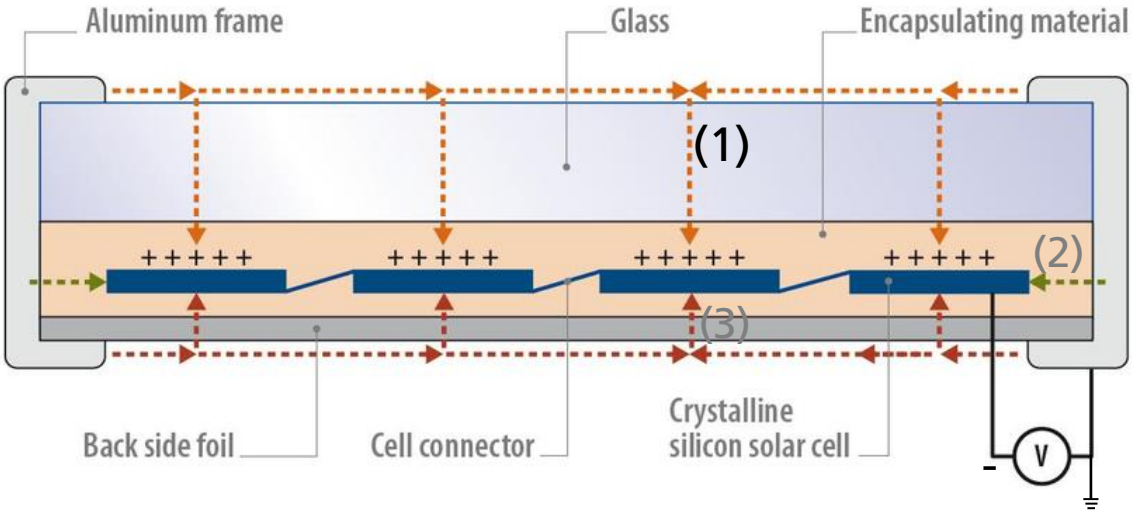
Potential-induced degradation (PID) of c-Si solar cells

- PID results in a very strong power decrease of c-Si solar modules
- Massive shunting solar cells → this prevalent type of PID is called "PID-s"
- Responsible: leakage current – dependent on voltage and temperature



Leakage current path
(1) throgh glass/polymer (predominant)
(2) lateral through polymer foil (minor contributions)
(3) through backsheet (extraneous to PID-s)

Source:
UL International Germany

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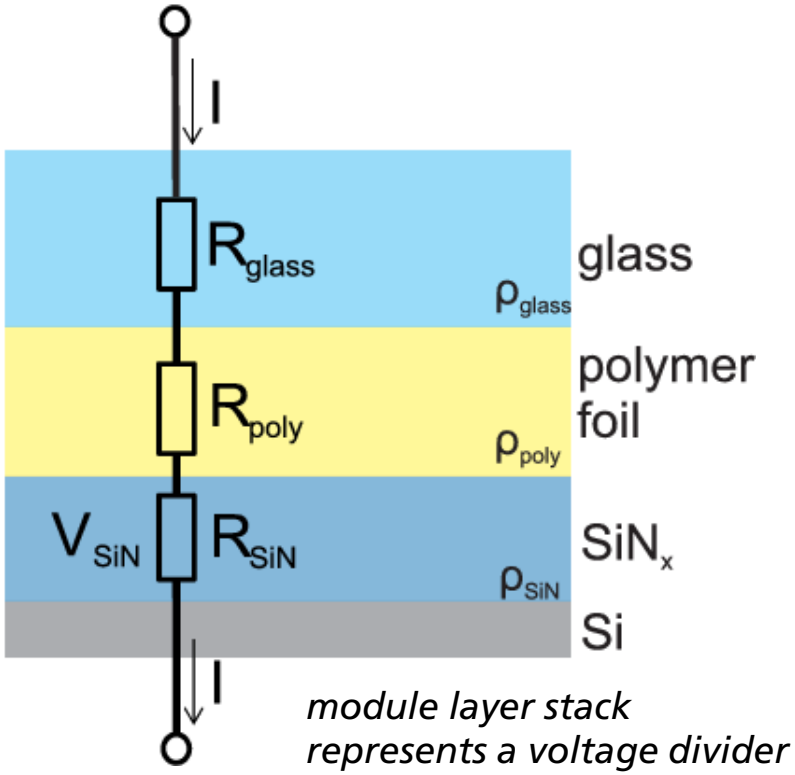
Electrical model for PID

- Special glass sorts cause resistance against PID-s
- Some polymer foils cause resistance against PID-s

→ Leakage current *I* influenced by resistivity of glass and polymer

- PID-s resistance also achieved through low resistivity of SiN_x layer (high refractive index)
- Voltage across SiN_x layer: V_{SiN} is the critical parameter

→ Voltage divider model



module layer stack represents a voltage divider upon leakage currents

$$V_{SiN} = I \cdot R_{SiN}$$

[1] Naumann, V.; Ilse, K.; Hagendorf, C.: On the discrepancy between leakage currents and potential-induced degradation of crystalline silicon modules, *Proceedings 28th European Photovoltaic Solar Energy Conference and Exhibition,* 2013, 2994-2997

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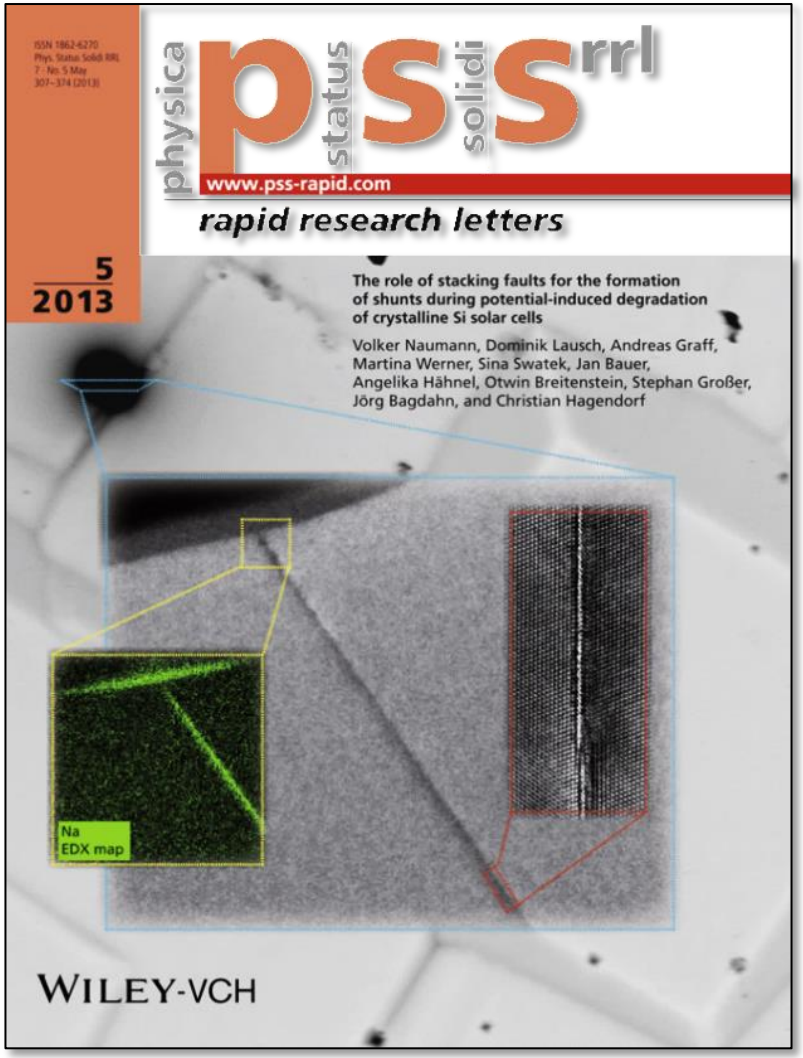
Physical root cause for PID-s



- High voltage across SiN_x layer causes drift of alkali ions
- Decoration of extended defects in Si {111} planes → "stacking faults" from the SiN_x/Si interface

→ High electric conductivity of stacking faults → shunting

→ Assessment of shunt resistance R_P to quantify PID-s

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Part 2: Experimental setup for PIDcon cell testing

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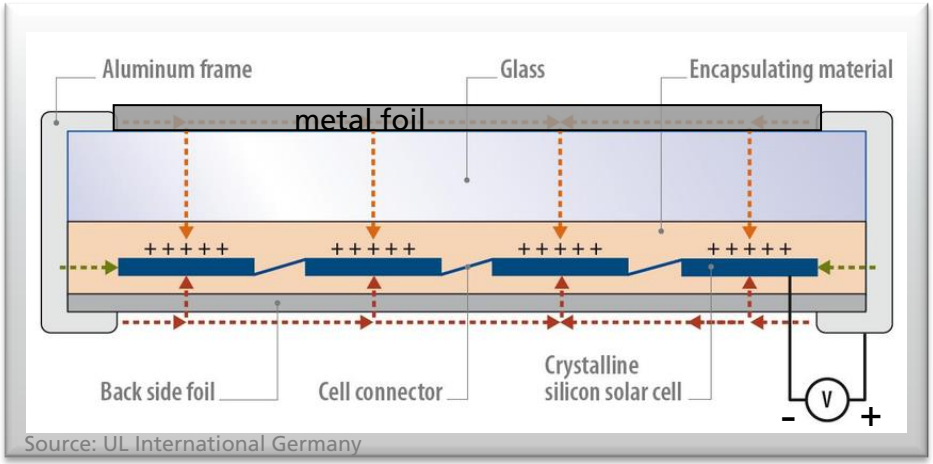
PID testing using the standard module test (for comparison)

- On module level: PID test standard available: **IEC 62804-1 TS**:

  "Photovoltaic (PV) modules – Test methods for the detection of potential-induced degradation – Part 1: Crystalline silicon"

- Procedure (b): Contacting surface by covering with grounded, electrically conducting electrode in controlled environment



Parameters:

- Module with Al foil in environmental chamber
- Temperature: 25 °C (up to 60 °C)
- Dry conditions
- Duration: 168 hours
- Voltage: 1000 or 1500 V (depending on module type)

But: Long test time | Elaborate module manufacturing needed | Expensive equipment/operation

→ Quick PID test on cell level attractive

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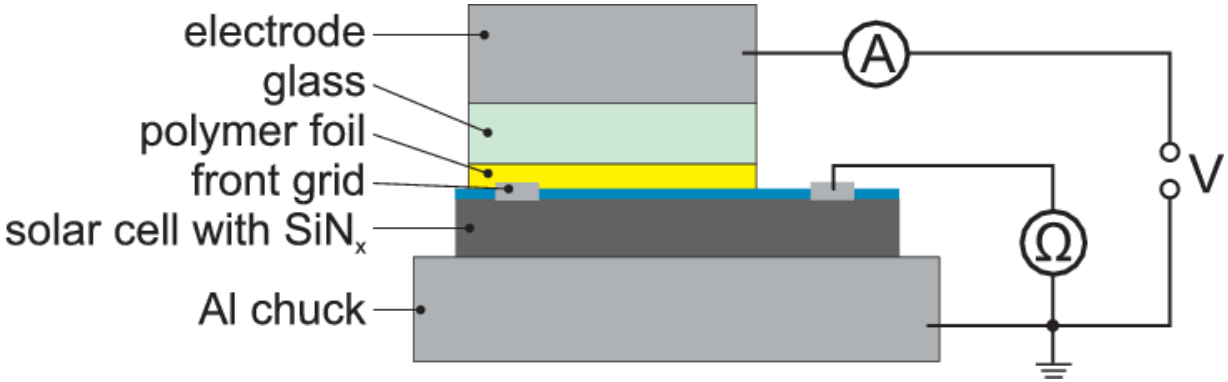
PIDcon cell test

Setup

- Module-like layer stack of solar cell + polymer foil + glass between two metal electrodes
- High positive voltage at upper electrode
  → voltage equivalent to PID in module
- Bottom electrode (ground) is heated
- Acquisition of shunt resistance as a function of time

PIDcon device (Freiberg Instruments)



Schematic of the PIDcon test setup

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PIDcon cell test
Materials

Solar cell:

- Si solar cell, minimum size 125 x 125 mm
- Front side contact grid with at least two busbars
- Original shunt resistance (before PID test) between some 10 Ω and 15 kΩ

Polymer foil:

- EVA foil (d < 0.5 mm) with resistivity ~10^{13} Ωcm (e.g. Bridgestone EVASKY)

Glass:

- Float glass, according to DIN EN 572-2, with low iron content
- Thickness: 3…4 mm
- Pieces of 10 x 10 cm²

PIDcon cell test
Test conditions

Preparation (according to SEMI standard)*:

- Stack EVA and glass (both 10 x 10 cm, square format) on solar cell, well aligned to top electrode
- Pre-lamination of the layer stack (in-situ option): 20 min @150 °C

Standard test conditions:

- Voltage: 1000 V
- Temperature: 85 °C
- Test duration: at least 4 hours
- Dry conditions, no use of water

* SEMI Draft Document 5889, NEW STANDARD: TEST METHOD ON CELL LEVEL FOR POTENTIAL-INDUCED DEGRADATION SUSCEPTIBILITY OF SOLAR CELLS AND MODULE ENCAPSULATION MATERIALS, Jan. 2016.

Part 3: Example results

Four-fold PIDcon test device at Fraunhofer CSP

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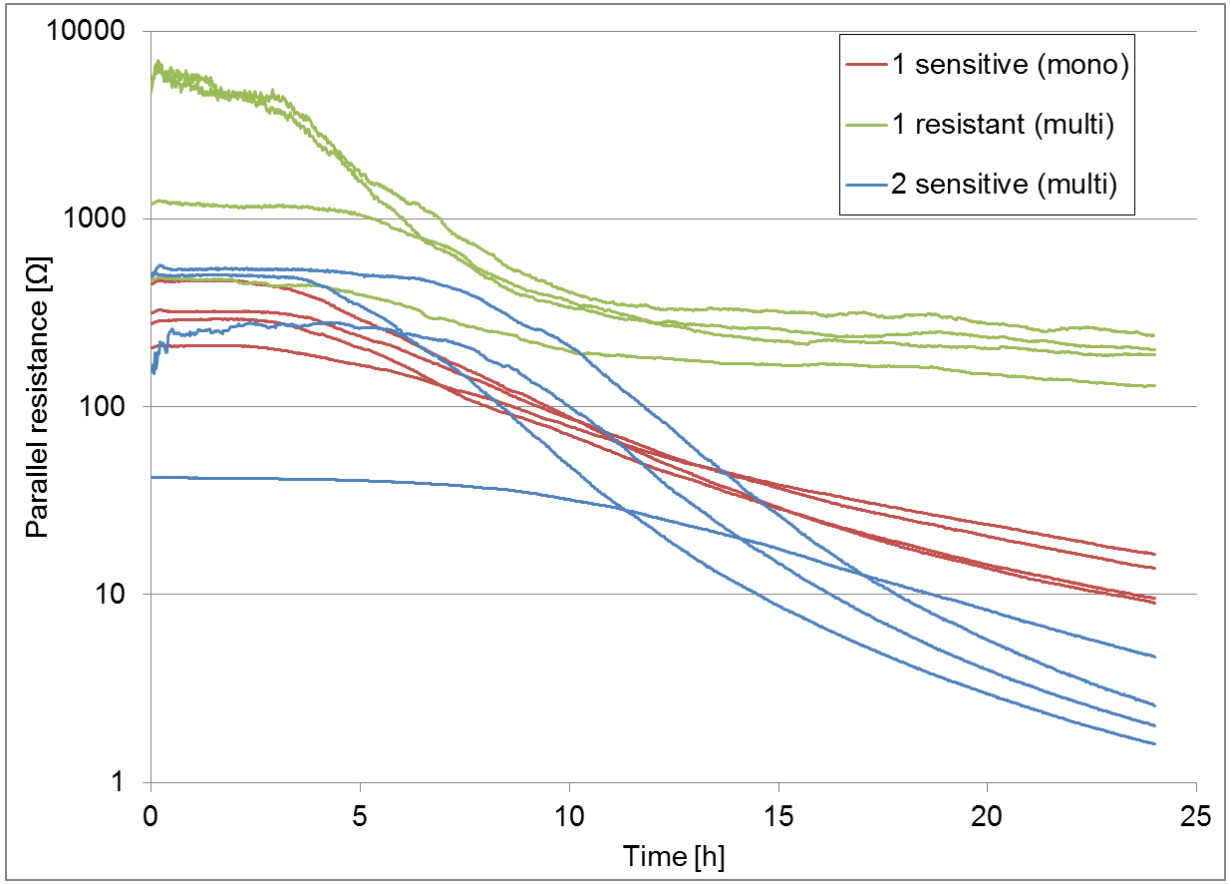
Results of a PID cell test series

- PID test of three Si solar cell types at 60 °C and 1000 V
- Plot of parallel resistance (shunt) as a function of PID test time



- Initial R_p value depends on cell process
- R_p is reciprocal of shunting degree (very sensitive to minor current variations at high R_p levels)

→ Low R_p means high currents through shunts (PID-shunts)

The three cell types show significant differences in the progress of shunting due to PID-s with good repeatability.

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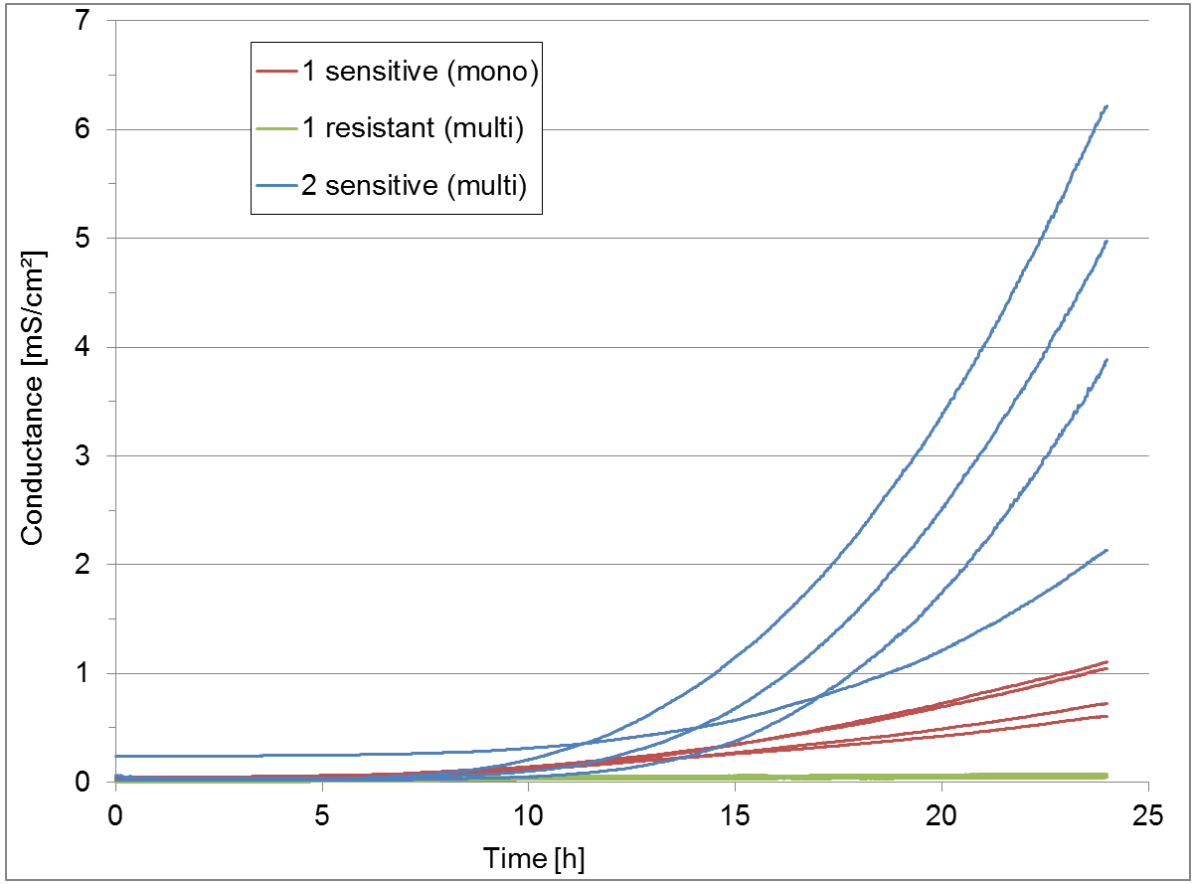
Results of a PID cell test series

- Plot of conductance (conductance = 1 / parallel resistance / stressed area)



- Conductance is proportional to current losses through shunts and (in first approx.) proportional to power loss at mpp

→ Power losses take effect first at very low R_p values

Cell type '2 sensitive' shows up to 6x of the power loss of cell type '1 sensitive'. Cell type '1 resistant' exhibits no power loss due to PID-s.

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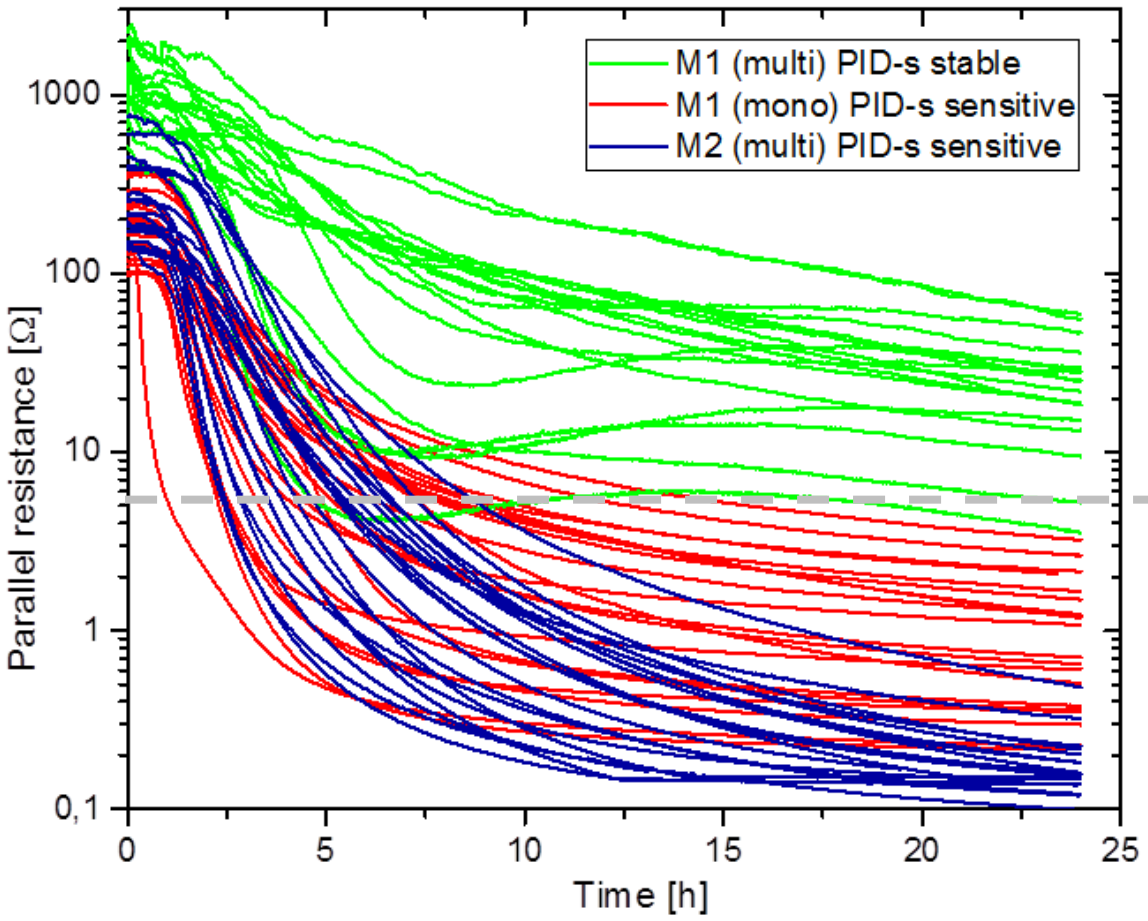
Extensive PID cell test series

- PID test of the same three Si solar cell types at 85 °C and 1000 V



> 5% power loss

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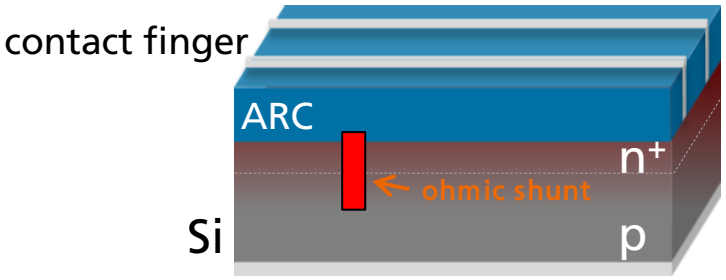
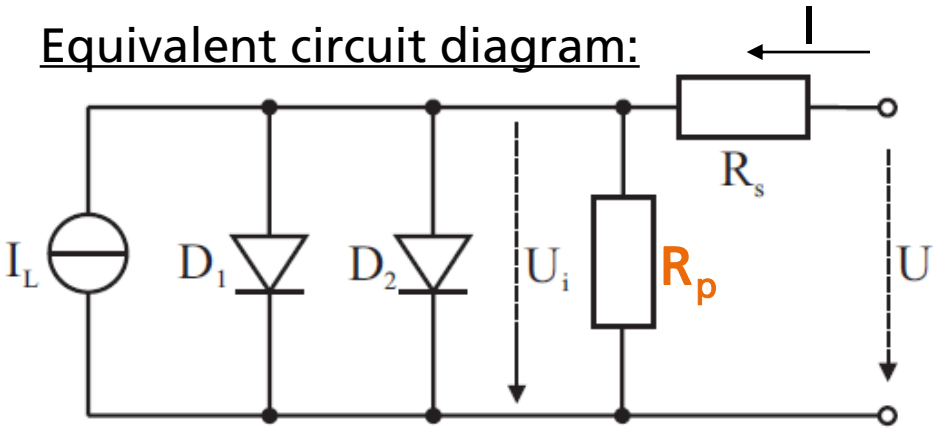
Power loss due to PID-s

Solar cell:



Equivalent circuit diagram:

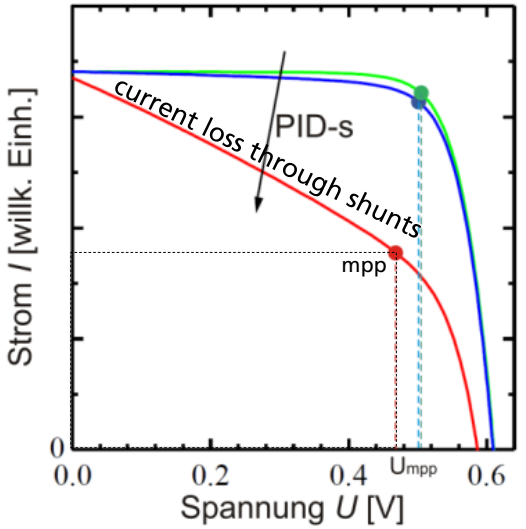


Two-diode-model:

$$I = I_{D1}(U_i) + I_{D2}(U_i) + \frac{U_i}{R_p} - I_L \quad , \quad U_i = U - IR_s$$

current loss through shunts;
max.-power-point: $U_i = U_{mpp}$

I-V curves under illumination:



[1]

- Approximation: power loss ΔP is proportional to current loss through shunts:

$$\Delta P \cong U_{mpp} \times \frac{U_{mpp}}{R_p}$$

relative power loss:

$$\frac{\Delta P}{P} \cong \frac{1}{I_{mpp}} \times \frac{U_{mpp}}{R_p}$$

[1] after: H. Nagel et al., Proc. 26th EU-PVSEC (2011), 3107–3112.

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